

07/20/00

U.S. PTO

Express Mail Label No.

# UTILITY PATENT APPLICATION TRANSMITTAL (Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.  
TI-23686-1

Total Pages in this Submission  
32

## TO THE ASSISTANT COMMISSIONER FOR PATENTS

Box Patent Application  
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

**INTEGRATED CIRCUIT HAVING INDEPENDENTLY FORMED ARRAY AND PERIPHERAL ISOLATION DIELECTRICS**

and invented by:

**CETIN KAYA**

JC836 U.S. PTO  
09/620649

07/20/00

If a CONTINUATION APPLICATION, check appropriate box and supply the requisite information:

☐ Continuation ☒ Divisional ☐ Continuation-in-part (CIP) of prior application No.: 09/168,047

Which is a:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.:

Which is a:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.:

Enclosed are:

### Application Elements

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having 23 pages and including the following:
  - a. ☒ Descriptive Title of the Invention
  - b. ☐ Cross References to Related Applications (if applicable)
  - c. ☐ Statement Regarding Federally-sponsored Research/Development (if applicable)
  - d. ☐ Reference to Microfiche Appendix (if applicable)
  - e. ☒ Background of the Invention
  - f. ☒ Brief Summary of the Invention
  - g. ☒ Brief Description of the Drawings (if drawings filed)
  - h. ☒ Detailed Description
  - i. ☒ Claim(s) as Classified Below
  - j. ☒ Abstract of the Disclosure

# UTILITY PATENT APPLICATION TRANSMITTAL (Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.  
TI-23686

Total Pages in this Submission  
32

## Application Elements (Continued)

3. ☒ Drawing(s) (when necessary as prescribed by 35 USC 113)
- a. ☐ Formal                      Number of Sheets \_\_\_\_\_
- b. ☒ Informal                      Number of Sheets 5
4. ☒ Oath or Declaration
- a. ☐ Newly executed (original or copy)                      ☐ Unexecuted
- b. ☒ Copy from a prior application (37 CFR 1.63(d)) (for continuation/divisional application only)
- c. ☒ With Power of Attorney                      ☐ Without Power of Attorney
- d. ☐ DELETION OF INVENTOR(S)  
Signed statement attached deleting inventor(s) named in the prior application,  
see 37 C.F.R. 1.63(d)(2) and 1.33(b).
5. ☒ Incorporation By Reference (usable if Box 4b is checked)  
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied  
under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby  
incorporated by reference therein.
6. ☐ Computer Program in Microfiche (Appendix)
7. ☐ Nucleotide and/or Amino Acid Sequence Submission (if applicable, all must be included)
- a. ☐ Paper Copy
- b. ☐ Computer Readable Copy (identical to computer copy)
- c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

## Accompanying Application Parts

8. ☐ Assignment Papers (cover sheet & document(s))
9. ☐ 37 CFR 3.73(B) Statement (when there is an assignee)
10. ☐ English Translation Document (if applicable)
11. ☐ Information Disclosure Statement/PTO-1449                      ☐ Copies of IDS Citations
12. ☐ Preliminary Amendment
13. ☒ Acknowledgment postcard
14. ☐ Certificate of Mailing
- ☐ First Class                      ☐ Express Mail (Specify Label No.): \_\_\_\_\_

**UTILITY PATENT APPLICATION TRANSMITTAL**  
**(Large Entity)**

*(Only for new nonprovisional applications under 37 CFR 1.53(b))*

Docket No.  
**TI-23686**

Total Pages in this Submission  
**32**

**Accompanying Application Parts (Continued)**

15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☐ Additional Enclosures *(please identify below):*

**Fee Calculation and Transmittal**

**CLAIMS AS FILED**

For	#Filed	#Allowed	#Extra	Rate	Fee
Total Claims	9	- 20 =	0	x \$18.00	\$0.00
Indep. Claims	1	- 3 =	0	x \$78.00	\$0.00
Multiple Dependent Claims (check if applicable) <input type="checkbox"/>					\$0.00
BASIC FEE					\$690.00
OTHER FEE (specify purpose)					\$0.00
TOTAL FILING FEE					\$690.00

- ☐ A check in the amount of \_\_\_\_\_ to cover the filing fee is enclosed.
- ☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. 20-0668 as described below. A duplicate copy of this sheet is enclosed.
- ☒ Charge the amount of \$690.00 as filing fee.
- ☒ Credit any overpayment.
- ☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).

*Signature*

**Jay M. Cantor**  
**Reg. No. 19906**  
**(202) 639-7713**

Dated:

cc:

## 5

This invention relates generally to the field of electronic devices, and more particularly, to an integrated circuit having independently formed array and peripheral isolation dielectrics.

BACKGROUND OF THE INVENTION

One type of modern nonvolatile memory is the EPROM or EEPROM device that uses floating gate structures. These floating gate memory structures may be integrated into a floating gate array which facilitates interface between the memory cells, control circuitry and high-voltage power sources. The memory cells use channel hot electrons for programming from the drain side and use Fowler-Nordheim tunneling for erasure from the source side. Due to the high voltages frequently used to program and erase the cells, high-voltage peripheral transistors may be implemented to provide an interface between a high-voltage source and the memory cells of the floating gate array. The control logic circuitry of the floating gate array typically functions with a lower operating voltage. Low-voltage peripheral transistors may be implemented to provide the logic circuitry for the array.

It is often desirable to fabricate peripheral transistors and the floating gate memory cells on a common semiconductor substrate. To ensure that each cell operates independently, regions of isolation dielectric may be formed between cells to electrically isolate the gates from one another. Typically, the isolation dielectrics for the memory cells are formed at the same time and are of the same construction as the isolation dielectrics for the periphery<sup>cl</sup> transistors. In addition, to ensure appropriate coupling coefficients, the distal ends of floating gates in the memory cell area are made to overlap the isolation dielectric. The proper voltage applied to the control gate is proportional to the coupling coefficient of the device. Providing overlap of the ends of the floating gates over the isolation dielectric increases the coupling coefficient, allowing for a lower control gate voltage.

5  
10  
15

20  
25  
30

5

10

15

SUMMARY OF THE INVENTION

5 In accordance with the teachings of the present invention, an integrated circuit having independently formed array and peripheral isolation dielectrics is provided that substantially eliminates or reduces the disadvantages associated with the prior techniques and processes.

10 According to one embodiment of the present invention, a method of forming an integrated circuit comprises forming a first dielectric layer disposed outwardly from a semiconductor substrate and forming a first intermediate structure outwardly from the first dielectric layer. The first intermediate structure comprises a floating gate layer disposed outwardly from the first dielectric layer, 15 a second dielectric layer disposed outwardly from the floating gate layer and a first polysilicon layer disposed outwardly from the second dielectric layer. Next, regions of the first intermediate structure are removed to form at least one gate stack disposed outwardly from the substrate. 20 After the formation of the gate stacks, at least one dielectric isolation region is formed between two gate stacks.

25 The invention has several important technical advantages. The dielectric isolation regions of the array are formed independently of the peripheral dielectric regions. Peripheral dielectric regions may be formed to a desired thickness for high voltage devices, while array dielectric regions may be scaled to minimize cell size. Additionally, the invention eliminates overlap between the 30 distal ends of the floating gates and the isolation dielectric residing between the gates. The area of substrate supporting each floating gate may be maintained or increased despite the scaling of the floating gate width. A good read current is, therefore, maintained



10

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the teachings of the present invention may be acquired by referring to the accompanying figures in which like reference numbers indicate like features and wherein;

FIGURE 1 is a cross-sectional view of a portion of one embodiment of an integrated circuit having independently formed array and peripheral isolation dielectric regions according to the teachings of the present invention;

FIGURE 2 is a cross-sectional view of a portion of another embodiment of an integrated circuit having independently formed array and peripheral isolation dielectric regions according to the teachings of the present invention;

FIGURES 3a-3d are a series of cross sectional views showing a portion of a partially completed integrated circuit having independently formed array and peripheral isolation dielectric regions constructed according to the teachings of the present invention; and

FIGURES 4a-4d are a series of cross-sectional views showing a portion of a partially completed integrated circuit having independently formed array and peripheral isolation regions completed according to the teachings of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

FIGURE 1 is a cross-sectional view of a portion of an integrated circuit 10 having independently formed array and peripheral isolation dielectric regions according to the teachings of the present invention. Integrated circuit 10 comprises a semiconductor substrate 12. A first dielectric layer 20 may be disposed outwardly from an array region 11 of integrated circuit 10. A peripheral dielectric layer 60 may be disposed outwardly from a peripheral region 13 of integrated circuit 10. First dielectric layer 20 and peripheral dielectric layer 60 may comprise, for example, layers of oxide. Other dielectric materials besides oxide may be used to form first and peripheral dielectric layers 20 and 60. First dielectric layer 20 may form a tunnel oxide layer for a floating gate array of memory cells subsequently formed in array region 11. Peripheral dielectric layer 60 may form a gate oxide layer for peripheral transistors subsequently formed in peripheral region 13.

Gate stacks 22 are disposed outwardly from substrate 12 and are separated from substrate 12 by first dielectric layer 20. Each gate stack 22 comprises a floating gate body 24 disposed outwardly from first dielectric layer 20. Each gate stack 22 further comprise a first polysilicon body 26 disposed outwardly from floating gate body 24 and separated from floating gate body 24 by a second dielectric region 28. Second dielectric region 28 may comprise any suitable dielectric material or combination of dielectric materials. Second dielectric region 28 may comprise, for example, oxide, nitride or a heterostructure comprising alternate layers of oxide and nitride. Dielectric isolation regions 30 may reside between gate stacks 22. Each dielectric isolation region may comprise an isolation oxide layer 32 disposed outwardly from the sidewalls of

To maximize the areas of substrate supporting gate stacks 22 and to minimize device topography, it may be desirable to form integrated circuit 10 such that floating gates 24 do not overlap dielectric isolation regions 30, as illustrated. Eliminating overlap between floating gate 24 and dielectric isolation regions 30, however, decreases the coupling coefficient of the device. Where no overlap exists, the capacitance between floating gate 24 and substrate 12 is comparatively greater because there is less dielectric separating the regions. An increase in the capacitance between floating gate 24 and substrate 12 without a corresponding increase in the capacitance between floating gate 24 and first polysilicon body 26 results in a reduced coupling coefficient.

To maintain a high coupling coefficient, it becomes desirable to increase the capacitance between floating gate 24 and first polysilicon body 26. The capacitance between floating gate body 24 and first polysilicon body 26 is inversely proportional to the thickness of second dielectric region 28 between them. By reducing the thickness of second dielectric region 28, the capacitance between the two gate bodies may be increased. The thickness of second dielectric region 28 may be reduced by an amount necessary to effect an increase in the floating gate/first polysilicon body capacitance which is equal to the increase in the gate/substrate capacitance caused by eliminating overlap with dielectric isolation regions 30. Second dielectric region 28 may be scaled, for example, to achieve a dielectric structure having a thickness of approximately 70 Å.

FIGURE 2 shows another method of increasing the capacitance between a floating gate 124 and a first polysilicon body 126 of an integrated circuit 100. The capacitance between floating gate body 124 and first polysilicon layer 126 is directly proportional to the surface area of these two bodies. The capacitance between the two gate bodies may, therefore, be increased by increasing the surface area of one or both structures. The effective surface area of floating gate body 124 and first polysilicon body 126 may be increased by forming a hemispherical grain poly layer 110 outwardly from floating gate 124. Hemispherical grain poly layer 110 creates a rough surface outwardly from floating gate 124. Forming second dielectric region 128 outwardly from hemispherical grain poly layer 110 creates a rough surface on second dielectric region 128 during its formation. The rough surface on second dielectric region 128, in turn, creates a rough surface on first polysilicon body 126 when it is formed. The rough surface of first silicon body 126 creates additional effective surface area between floating gate body 124 and first polysilicon body 126, which increases the capacitance between these bodies, resulting in a higher coupling coefficient.

In another embodiment (not explicitly shown), the outer surface of first polysilicon body 124 may be roughened rather than forming a separate hemispherical grain poly layer 110. In this embodiment, the outer surface of first polysilicon layer 124 may be made rough by altering the deposition parameters during formation of first polysilicon body 124. This embodiment results in the same rough surface exhibited by hemispherical grain poly layer 110, without the formation of a separate structural layer.

FIGURES 3A-3D are cross-sectional views of a portion of a partially completed integrated circuit having independently formed array and peripheral isolation dielectrics constructed according to the teachings of the present invention.

Depending on the application and fabrication techniques employed, integrated circuit 10 may, but need not comprise a plurality of trenches and a plurality of moats formed adjacent to the plurality of trenches in semiconductor substrate 12 (not explicitly shown). Trenches and moats may be formed at a variety of points in the fabrication process and by a variety of methods. For example, trenches and moats may be formed contemporaneously with the formation of gate stacks 22 using the same etch used to form gate stacks 22. In that case, the trenches may be filled with a dielectric similar to that used for dielectric isolation region 30 described with reference to FIGURE 1. Alternatively, trenches and moats may be formed by etching away regions of substrate 12 prior to formation of gate stacks 22. In that case, regions of trench dielectric may be disposed within the trenches to substantially fill the trenches. First dielectric layer 20 may then be formed outwardly from substrate 12.

FIGURE 3A shows integrated circuit 10 after formation of a first immediate structure 40 disposed outwardly from first dielectric layer 20. First dielectric layer 20 may be formed outwardly from substrate 12. As described above, trenches and moats may, but need not be formed in substrate 12 prior to formation of first dielectric layer 20. If trenches are formed at that point, regions of trench dielectric may be disposed within the trenches to fill the trenches. Next, floating gate layer 23 may be formed outwardly from first dielectric layer 20. Floating gate layer 23 may comprise, for example, polysilicon or



5  
10

15

20

25

30





may be formed by any suitable method, such as by deposition or thermal growth. If peripheral dielectric layer 60 is formed through thermal growth, its thickness may be greater in array region 11 than in peripheral region 13. This is due to doping of second polysilicon layer 50, which causes increased growth of thermally grown dielectrics. Peripheral dielectric layer 60 may comprise, for example, oxide or any other suitable dielectric or combination of dielectrics. Third polysilicon layer 70 may be disposed outwardly from peripheral dielectric layer 60. Third polysilicon layer 70 may later form gates of peripheral transistors of integrated circuit 10.

FIGURE 4D shows integrated circuit 10 after the formation of a gate 80 in peripheral region 13. Gate 80 may be formed, for example, by forming a peripheral gate pattern (not shown) outwardly from peripheral dielectric layer 60. The peripheral gate pattern may mask regions of third polysilicon layer 70 outwardly from peripheral region 13, leaving all other areas of third polysilicon layer 70 exposed. Peripheral gates 80 may be formed by etching exposed regions of third polysilicon layer 70 leaving peripheral gates 80 disposed outwardly from peripheral region 13. Sidewall spacers 90 may be formed outwardly from the sidewalls of peripheral gates 80 by any suitable method.

Although the present invention has been described in detail, it should be understood that various changes, substitutions, and alterations can be made hereto without departing from the spirit and scope of the invention as defined by the appended claims.

WHAT IS CLAIMED IS:

1. A method for forming an integrated circuit, comprising:

forming a first dielectric layer disposed outwardly from a semiconductor substrate;

forming a first intermediate structure comprising:

a floating gate layer disposed outwardly from the first dielectric layer;

a second dielectric layer disposed outwardly from the floating gate layer; and

a first polysilicon layer disposed outwardly from the second dielectric layer;

removing regions of the first intermediate structure to form at least one gate stack;

forming at least one dielectric isolation region after the formation of the gate stacks, wherein the at least one dielectric isolation region is disposed between two gate stacks.

2. The method of Claim 1, wherein forming a dielectric isolation region comprises:

growing an isolation oxide layer outwardly from the gate stacks;

depositing an isolation dielectric layer outwardly from and between the gate stacks; and

removing at least a portion of the isolation oxide layer and the isolation dielectric layer to expose at least an outer surface of the first polysilicon layer.

5

5

5

10

15

15

20

25

25

30

30

30

5

10

10

15

20

9. The method of Claim 1, wherein the floating gate layer comprises a rough outer surface.

25

10. The method of Claim 1, further comprising forming a peripheral dielectric layer outwardly from a peripheral region of the substrate, the peripheral region of the substrate disposed adjacent to a region of the substrate supporting the at least one gate stack.

5

5

5

10

15

20

20

25

34

12. An integrated circuit, comprising:

- a first dielectric layer disposed outwardly from a substrate;
- a plurality of gate stacks, each gate stack comprising:
  - a floating gate body disposed outwardly from the first dielectric layer;
  - a second dielectric region disposed outwardly from the floating gate body; and
  - a first polysilicon layer disposed outwardly from the second dielectric region; and
- a plurality of dielectric isolation regions disposed between the gate stacks, the dielectric isolation regions formed after the formation of the gate stacks.

13. The integrated circuit of Claim 12, wherein each dielectric isolation region comprises:

- an isolation oxide layer; and
- an isolation dielectric layer;

the dielectric isolation region formed by growing the isolation oxide layer outwardly from the gate stacks; depositing the isolation dielectric layer outwardly from and between the gate stacks; and removing at least a portion of the isolation oxide layer and the isolation dielectric layer to expose at least an outer surface of the first polysilicon layer.

14. The integrated circuit of Claim 12, wherein each dielectric isolation region comprises:

an isolation oxide layer; and

an isolation dielectric layer;

5 the dielectric isolation region formed by:

growing approximately 200 Å of oxide outwardly from the gate stacks;

depositing approximately 0.5 micrometers of oxide outwardly from and between the gate stacks; and

10 removing at least a portion of the isolation oxide layer and the isolation dielectric layer to expose at least an outer surface of the first polysilicon layer.

15 15. The integrated circuit of Claim 12, wherein the substrate comprises at least one trench disposed between two gate stacks; and

at least one moat disposed adjacent to the at least one trench and inwardly from the at least one gate stack.

20

16. The integrated circuit of Claim 15, wherein each dielectric isolation region comprises:

an isolation oxide layer; and

an isolation dielectric layer;

25 the dielectric isolation region formed by:

growing a layer of oxide outwardly from the gate stacks;

depositing a dielectric outwardly from and between the gate stacks and outwardly from the trenches in the substrate; and

30

removing at least a portion of the isolation oxide layer and the isolation dielectric layer to expose at least an outer surface of the first polysilicon layer.



5           18. The integrated circuit of Claim 12, wherein each gate stack further comprises a hemispherical grain poly layer disposed outwardly from the floating gate body.

20. The integrated circuit of Claim 12, further comprising:

a peripheral dielectric layer disposed outwardly from the second polysilicon layer and a peripheral region of the substrate, the peripheral region of the substrate disposed adjacent to a region of the substrate supporting the gate stacks;

25

INTEGRATED CIRCUIT HAVING INDEPENDENTLY FORMED  
ARRAY AND PERIPHERAL ISOLATION DIELECTRICS

ABSTRACT OF THE DISCLOSURE

5 The invention comprises a method of forming an integrated circuit, the method comprising: (1) forming a first dielectric layer disposed outwardly from a semiconductor substrate; (2) forming a first intermediate structure outwardly from the a dielectric layer, the first intermediate structure comprising a floating gate layer disposed outwardly from the first dielectric layer, a second dielectric layer disposed outwardly from the floating gate layer, and a first polysilicon layer disposed outwardly from the second dielectric layer; (3) removing regions of the first intermediate structure to form at least one gate stack disposed outwardly from the first dielectric layer; and (4) forming at least one dielectric isolation region after the formation of the gate stacks, wherein the at least one dielectric isolation region is disposed between two gate stacks.

10

15

09620649-072000

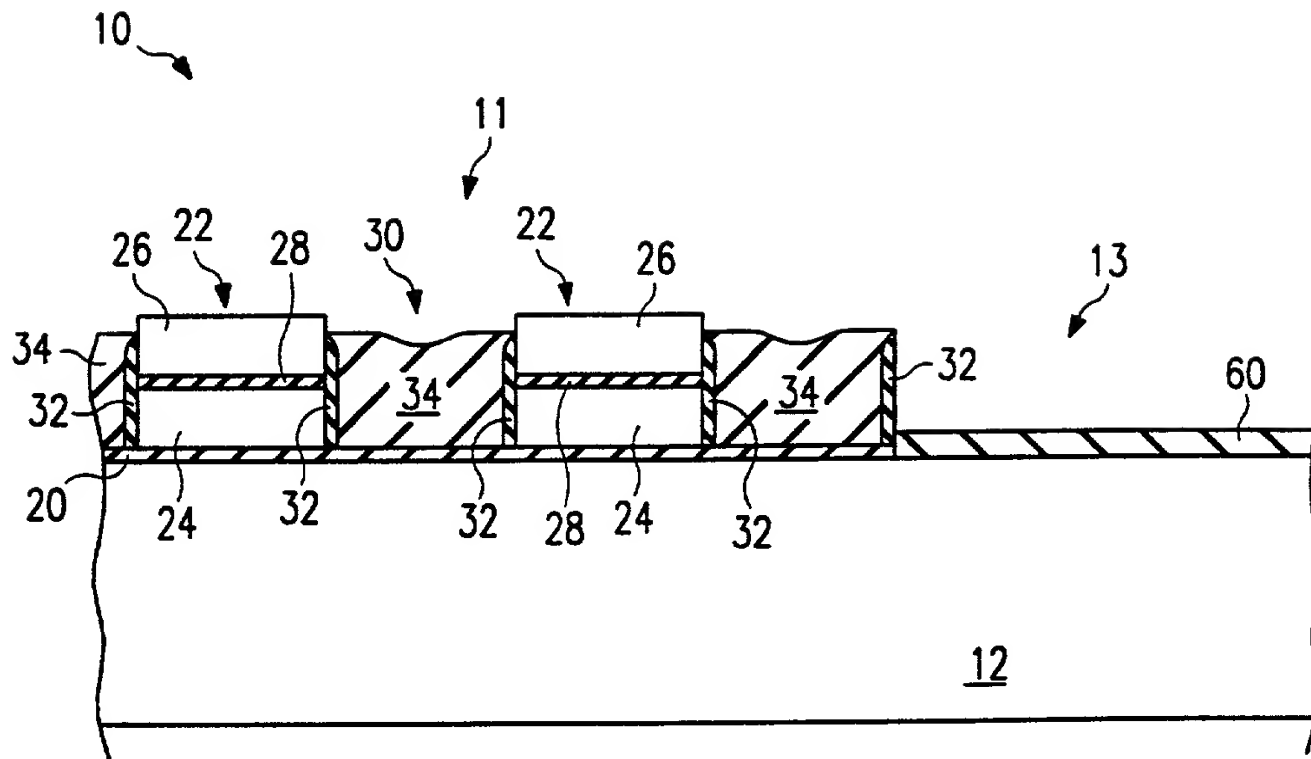


FIG. 1

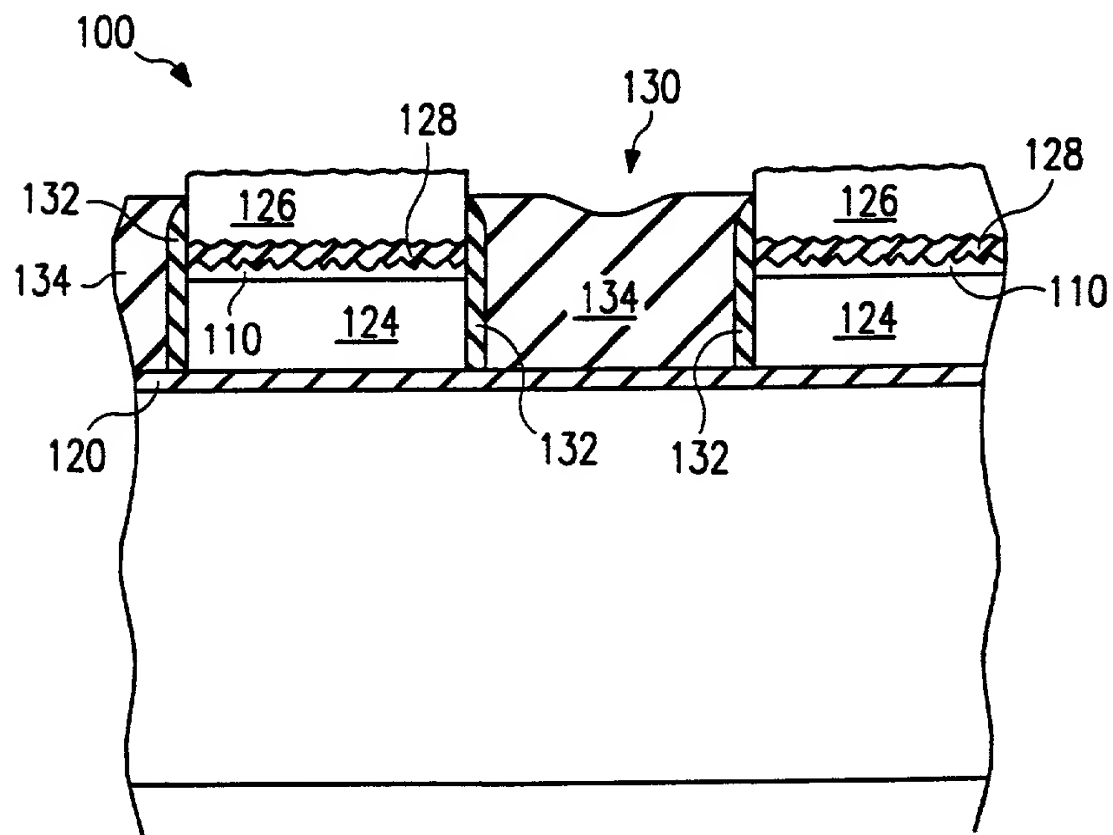


FIG. 2

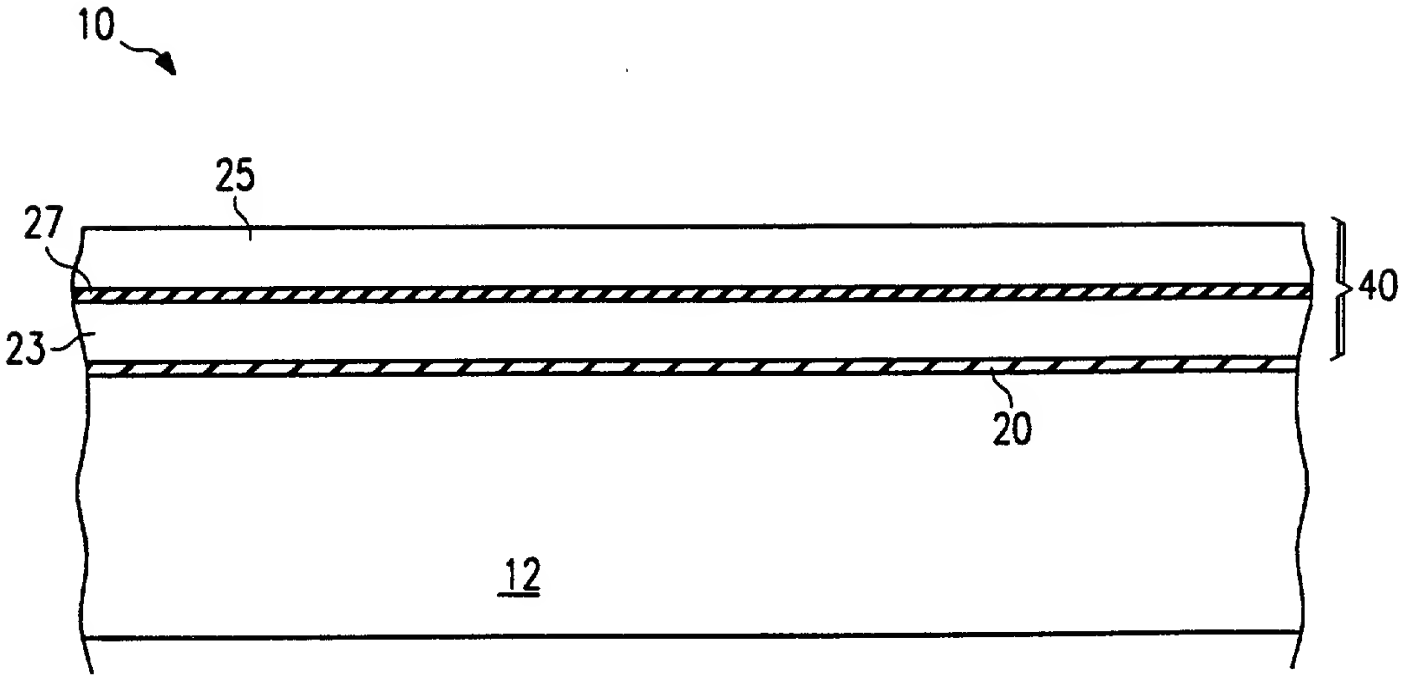


FIG. 3a

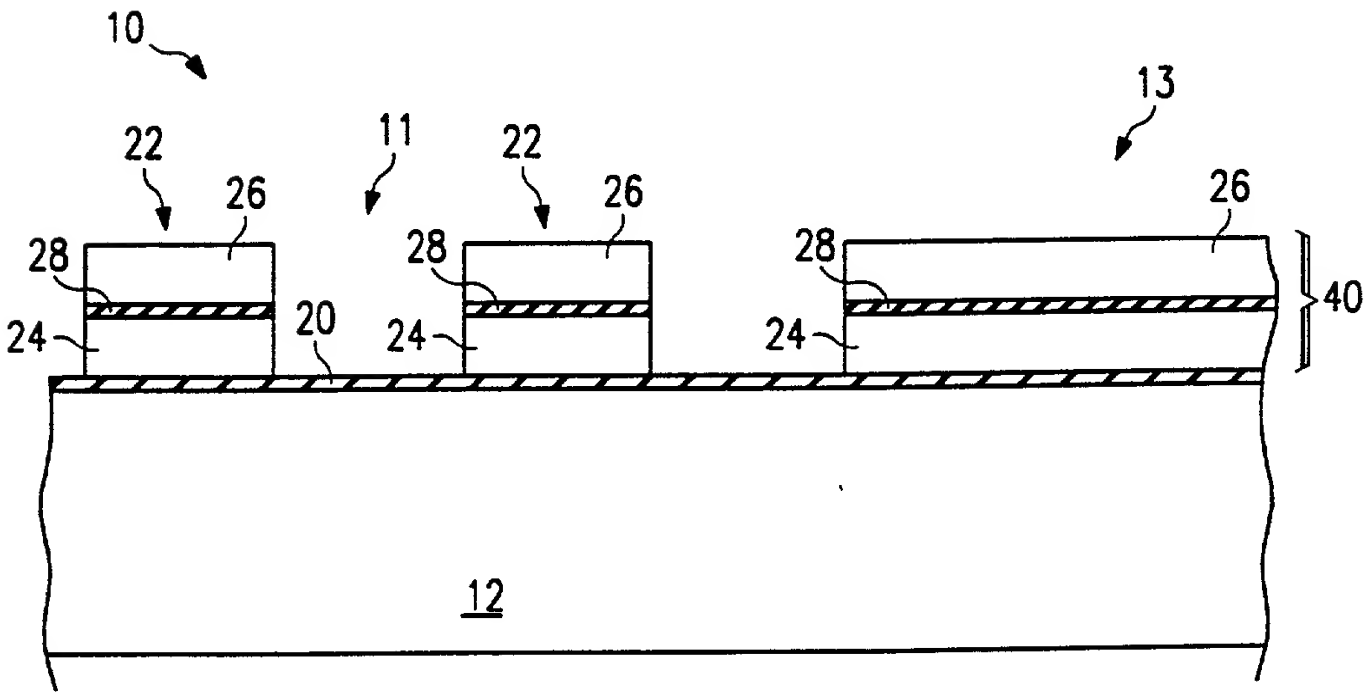


FIG. 3b

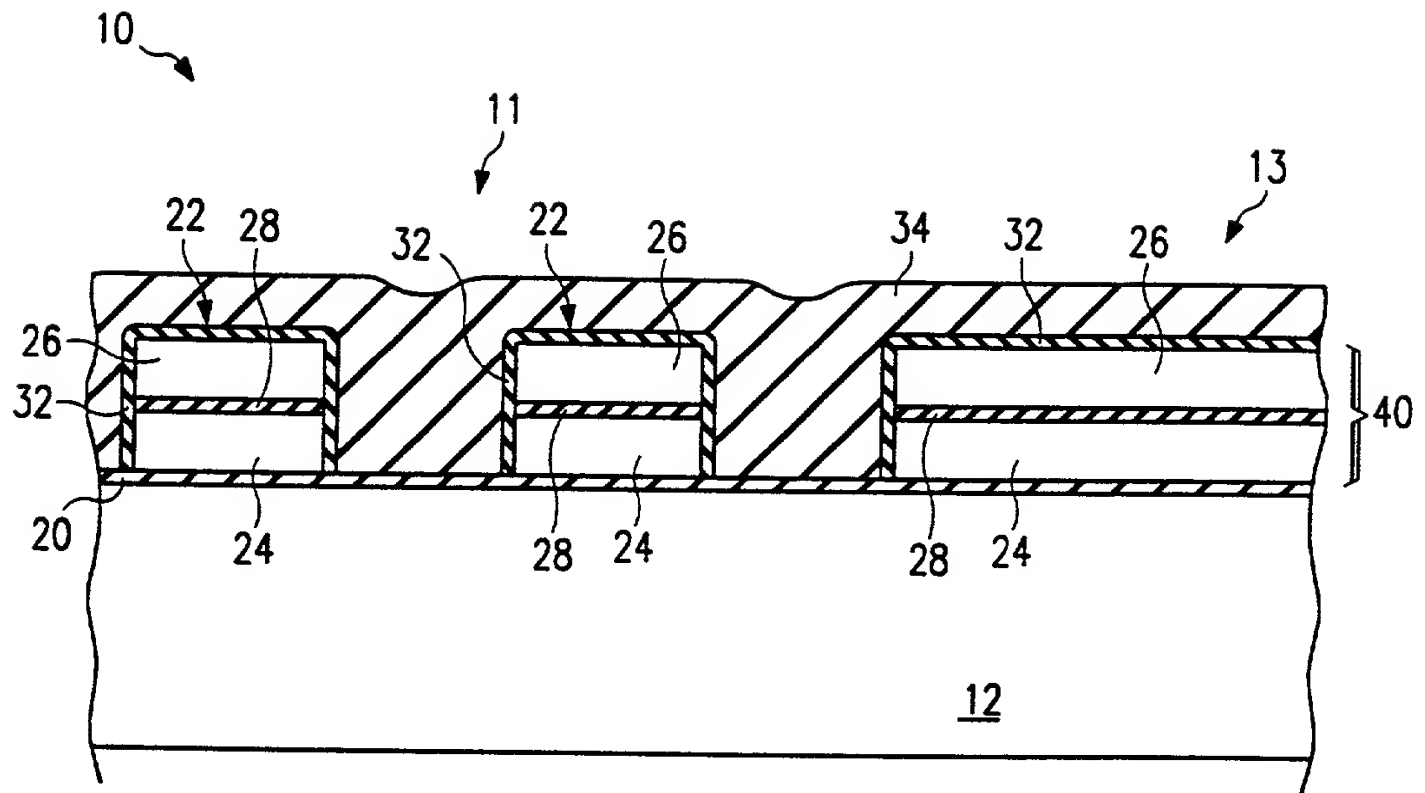


FIG. 3c

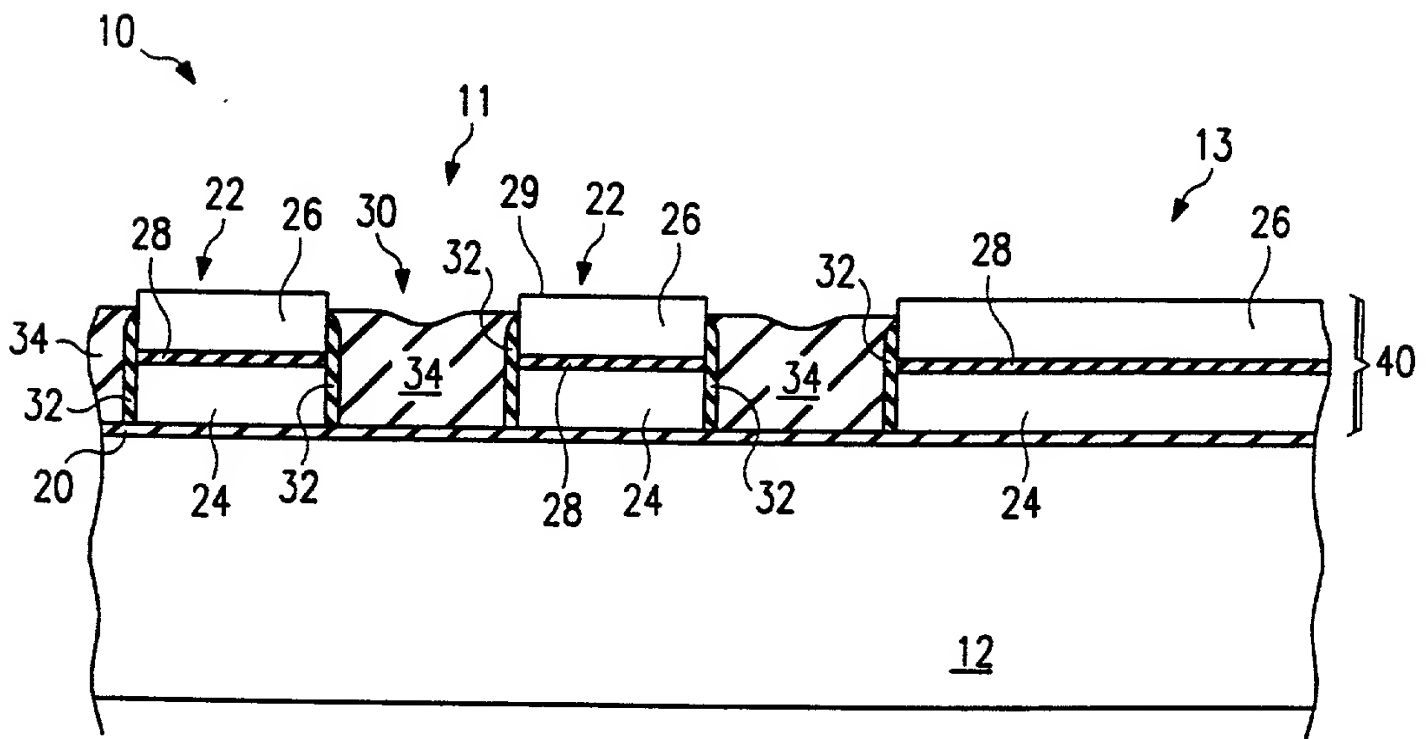


FIG. 3d

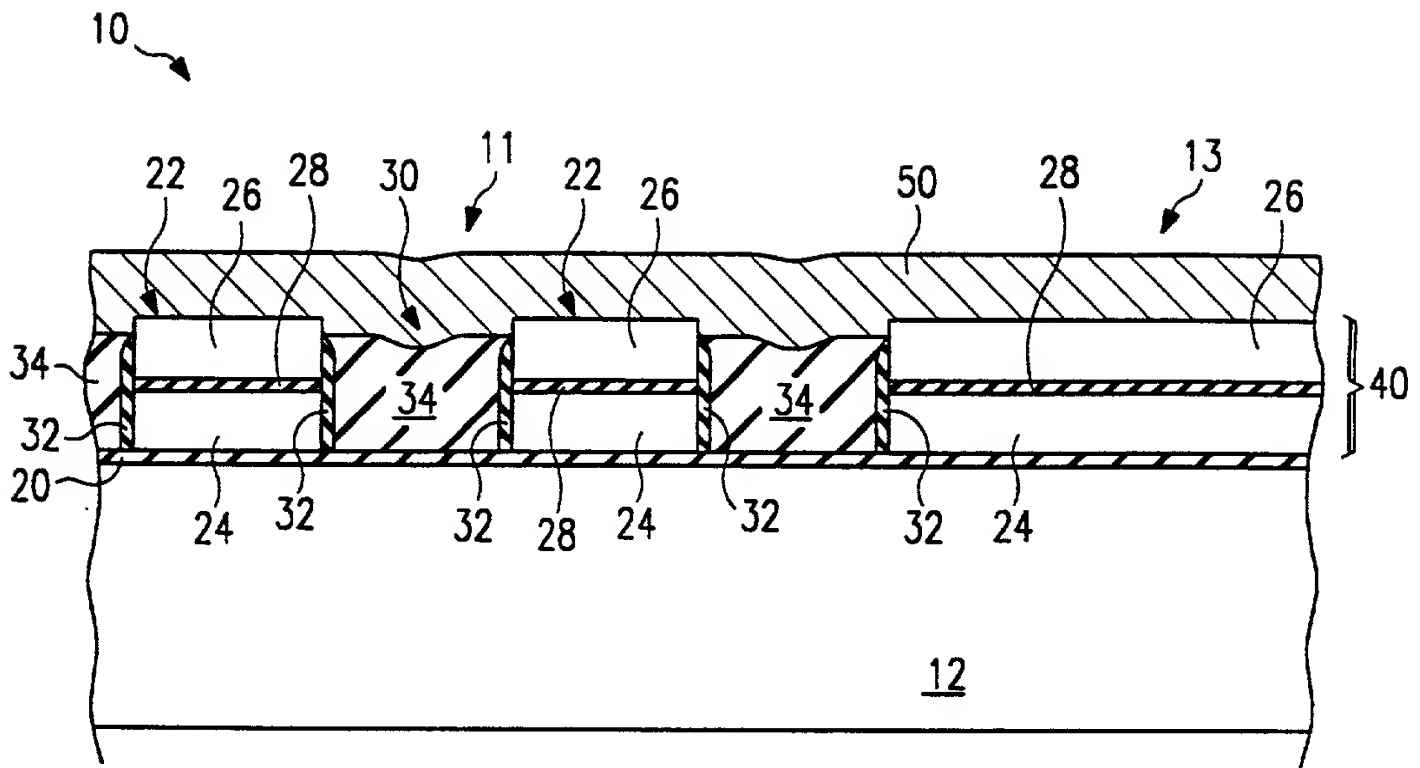


FIG. 4a

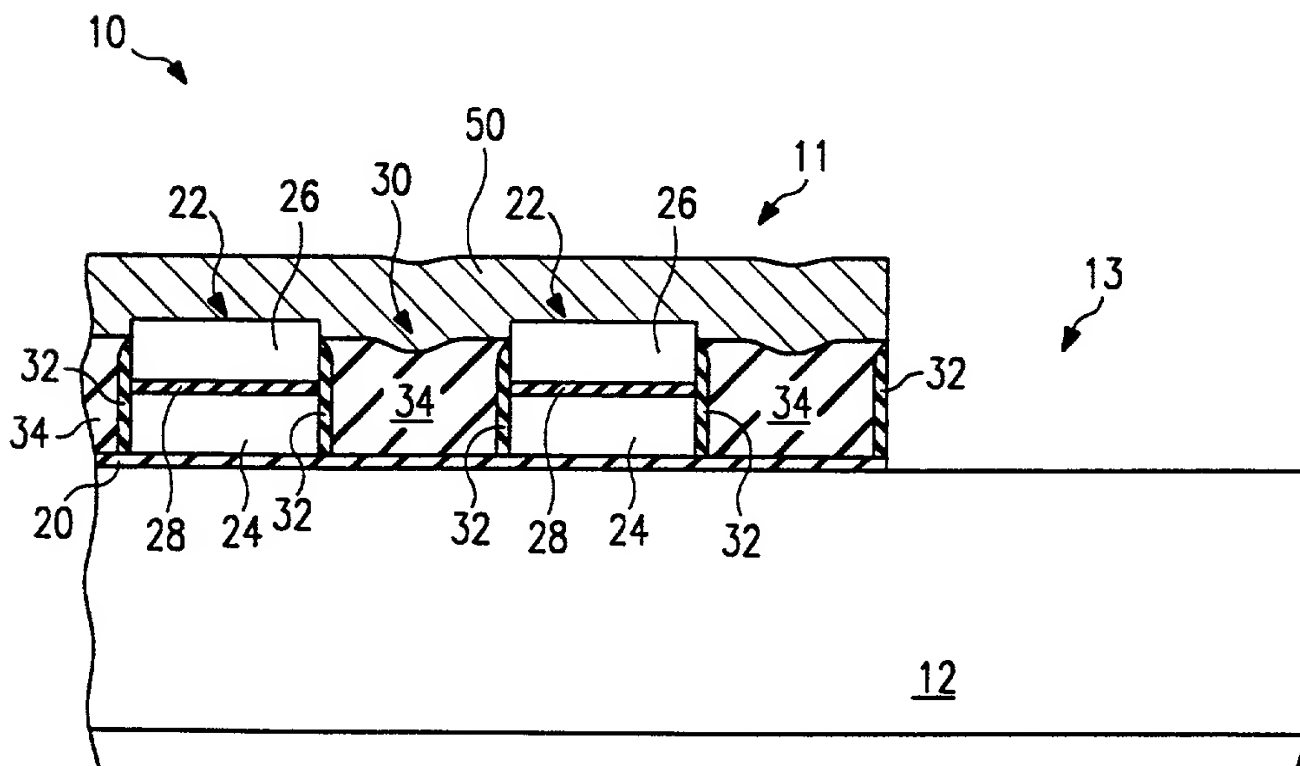


FIG. 4b

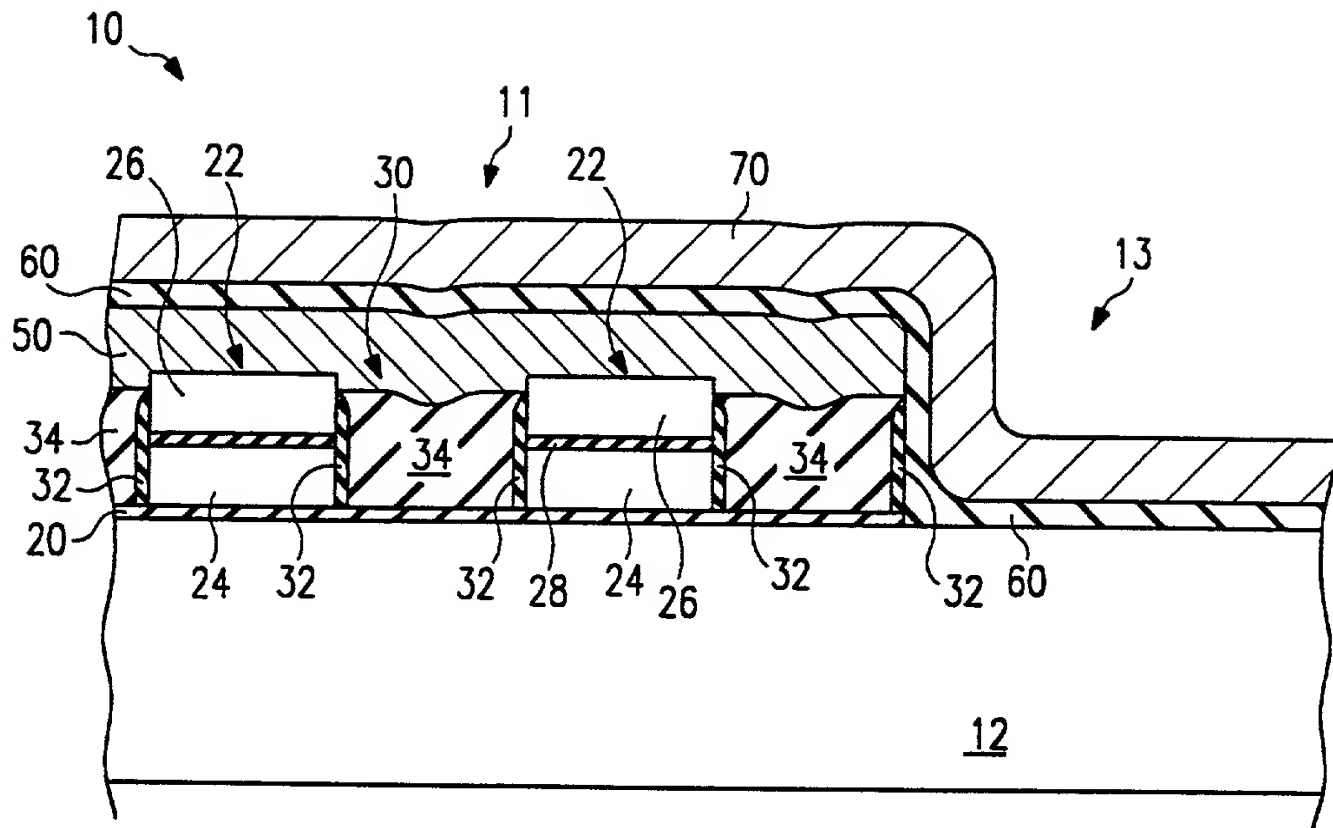


FIG. 4c

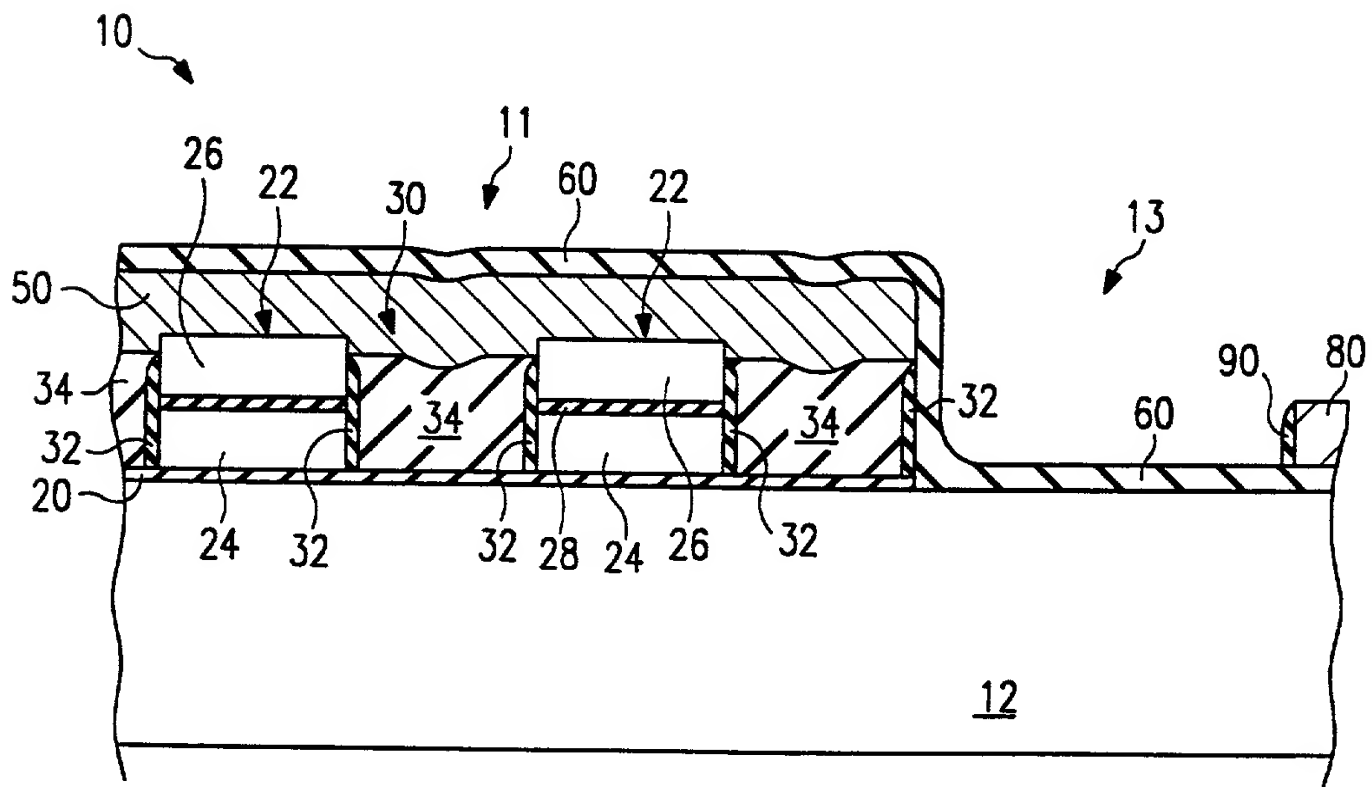


FIG. 4d





PATENT  
TI-23686

2

Please send correspondence to:

Jacqueline J. Garner, Esq.  
Texas Instruments Incorporated  
P. O. Box 655474, M/S 219  
Dallas, Texas 75265

and direct telephone calls to:

(973) 278-9697

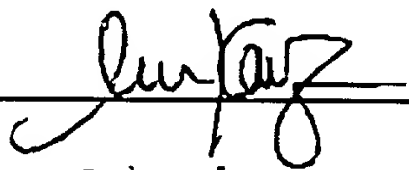
Name of Inventor:  
Residence & P.O.

Cetin (nmi) Kaya  
9900 Adleta Blvd., #1114  
Dallas, Texas 75243

Citizenship:

~~Turkey~~ U.S. CK 9/30/97

Signature of Inventor:

X 

Date:

K 9/30/97

09620649.071000